

IN THE CLAIMS:

1. A flash memory device comprising:
an array of non-volatile memory cells;
a clock signal connection to receive a clock signal comprising clock cycles;
a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections; and
command logic coupled to the array to provide two data access operations per clock cycle.
2. The flash memory device of claim 1 wherein the array of non-volatile memory cells is arranged in a plurality of addressable banks.
3. The flash memory device of claim 2 wherein each addressable bank contains addressable sectors of memory cells.
4. The flash memory device of claim 1 wherein the data connections are burst oriented and the control circuitry comprises means for starting data access at a selected location and continuing for a programmed number of locations in a programmed sequence
5. The flash memory device of claim 1 wherein the command logic includes control registers used to store data for memory operation control.
6. The flash memory device of claim 1 and further including sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines.

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7. The flash memory device of claim 1 and further including pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell.

8. The flash memory of claim 7 wherein the pre-charge circuitry pre-charges an active digit line that is coupled to a read memory cell to a voltage that is greater than a complementary digit line.

9. The flash memory of claim 7 wherein the pre-charge circuitry pre-charges the digit lines to a differential level using charge sharing.

10. The flash memory of claim 7 wherein the pre-charge circuitry pre-charges the digit lines to a differential level using a bias circuit.

11. A processing system comprising:

a processor; and
a rambus dynamic random access memory compatible flash memory device coupled to the processor, the memory device comprising:
an array of non-volatile memory cells;
a clock signal connection to receive a clock signal comprising clock cycles;
a rambus dynamic random access memory interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and
command logic coupled to the array to provide two data access operations per clock cycle starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

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11. The system of claim 10 wherein the processor generates flash memory compatible control signals.

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12. The system of claim 10 and further including pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell.

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13. The system of claim 10 wherein the processor is adapted to receive burst transmissions of data from the memory device.

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14. The system of claim 10 wherein the non-volatile memory device is a flash memory device.

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15. A processing system comprising:
a processor;
a single communication bus coupled to the processor;
a volatile memory device coupled to the single communication bus; and
a rambus dynamic random access memory (RDRAM) compatible flash memory device coupled to the single communication bus, the memory device comprising:
an array of non-volatile memory cells;
a clock signal connection to receive a clock signal comprising clock cycles; and
command logic coupled to the array to provide two data access operations per clock cycle following an RDRAM compatible format and starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

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16. The processing system of claim 15 wherein the volatile memory device and the RDRAM compatible flash memory device both respond to common command signals provided on the single communication bus.

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17. The processing system of claim 15 and further including:
sense amplifier circuitry coupled to the memory cells over bit lines, wherein the
sense amplifier circuitry detects a differential voltage between the bit lines; and
pre-charge circuitry coupled to pre-charge the bit lines to first and second
voltage levels to provide an initial differential voltage prior to sensing a memory cell.

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18. The processing system of claim 15 wherein the two data access operations per
clock cycle are performed on clock transitions.

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19. The processing system of claim 15 wherein the memory cells are floating gate
memory cells.

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20. The processing system of claim 15 wherein the processor generates computer
system commands.